

Amendment and Response Under 37 C.F.R. 1.116

Applicant: Michael Bauer et al.

Serial No.: 10/789,033

Filed: February 27, 2004

Docket No.: I431.103.101/FIN423US

Title: ELECTRONIC COMPONENT AND SEMICONDUCTOR WAFER, AND METHOD FOR PRODUCING THE SAME

REMARKS

The following remarks are made in response to the Final Office Action mailed January 8, 2007 and the Advisory Action mailed May 17, 2007. With this Response, claims 6-14 have been amended and claims 18-20 have been cancelled. Claims 6-14 remain pending in the application and are presented for reconsideration and allowance.

Election/Restriction

Section 2 of the Office Action characterized claims 18-20 as being directed to an invention that is independent or distinct from the invention originally claimed, referencing 37 CFR 1.142(b) and MPEP 821.03. Without going further into the merits of this characterization of claims 18-20, Applicants have cancelled claims 18-20 in an effort to move the application to allowance.

Drawings

Section 3 of the Office Action objected to the drawings under 37 CFR 1.83(a) specifically with regard to features recited in claims 4 and 6. Claim 4 has been cancelled. Claim 6 recites “the rear sides of the semiconductor chips are oriented virtually perpendicular to the top side of the circuit substrate.” This is illustrated, for example, in Figure 9, which shows rear sides of chips 6 oriented perpendicularly to the top surface 25 of the insulated substrate 35.

Applicants therefore respectfully request the objections to the drawings be withdrawn.

Specification

Section 4 of the Office Action objection to the specification with regard to claim 6. Claim 6 has been amended to provide antecedent basis for the *circuit substrate*. The specification provides ample disclosure of the circuit substrate.

Applicants thus believe the objection to the specification has been overcome.

Amendment and Response Under 37 C.F.R. 1.116

Applicant: Michael Bauer et al.

Serial No.: 10/789,033

Filed: February 27, 2004

Docket No.: I431.103.101/FIN423US

Title: ELECTRONIC COMPONENT AND SEMICONDUCTOR WAFER, AND METHOD FOR PRODUCING THE SAME

Claim Rejections under 35 U.S.C. § 112

Sections 5-6 of the Office Action rejected claim 4 under 35 U.S.C. § 112, first paragraph. Claim 4 has been cancelled, rendering this rejection moot.

Sections 7-8 of the Office Action rejected claims 4 and 6-14 under 35 U.S.C. § 112, second paragraph. Claim 4 has been cancelled. Claim 6 has been amended to correct an informal error, changing “semiconductor wafers” to – semiconductor chips – .

In view of the above, all of the rejections under 35 U.S.C. § 112 are believed to be overcome.

Claim Rejections under 35 U.S.C. § 102

Sections 9-11 rejected claims 4 and 5 under 35 U.S.C. § 102(b). Claims 4 and 5 have been cancelled, rendering their rejections moot.

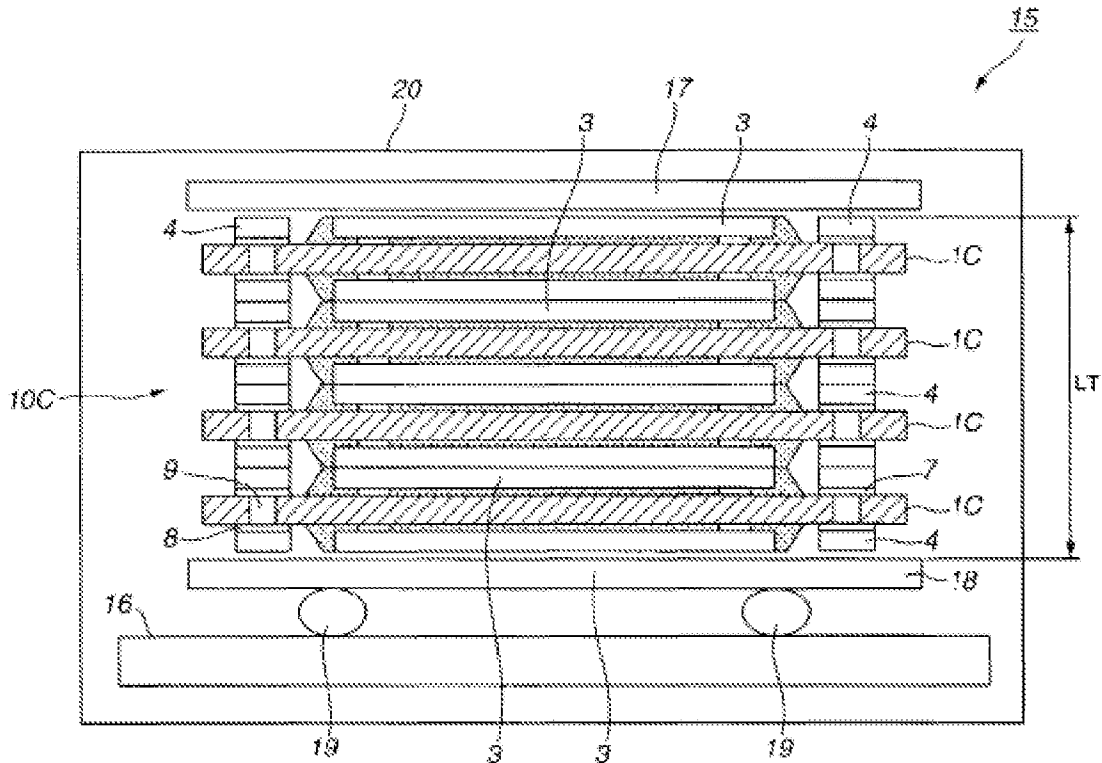
Claim Rejections under 35 U.S.C. § 103

The Office Action rejected claims 6-14 under 35 U.S.C. § 103 as allegedly being unpatentable over Nakajima JP 2002-299372 (“Nakajima”) in view of Koike et al. WO 03/012868 (equivalent to U.S. Patent No. 7,071,028, collectively “Koike”). Applicants respectfully traverse these rejections.

Claim 6 has been amended to recite “rear sides of the semiconductor *chips*”; and also to recite the top and rear sides of these chips being “oriented virtually perpendicular to a top side of the circuit substrate.” Claim 6 further clarifies that the top side includes an integrated circuit and the rear side is opposite the top side and parallel to the top side.

Claim 6 thus includes semiconductor chips oriented such that the top and rear sides of the semiconductor chips are oriented virtually perpendicular to a top side of the insulated substrate. The Office Action admits that Nakajima fails to disclose additional chips, but refers to Figures 6, 23 and 32 of Koike, stating Koike discloses chips “on an insulated substrate 18 such that the rear sides of the semiconductor wafers are oriented virtually perpendicular a top side of the substrate.”

Figure 32 of Koike is reproduced below.



Referring to Figure 32, Koike discloses a lower protective substrate 18. See col. 18, ll. 16-18. However, Figure 32 of Koike clearly shows the top and rear sides of the semiconductor chips 3 being oriented parallel to the top side of the substrate 18.

The Advisory Action states, “words of a claim must be given their plain meaning unless applicant has provided a clear definition in the specification.” As amended, claim 6 identifies the rear side as being opposite the top side having the integrated circuit. The specification clearly identifies integrated circuits on the top side, with the rear side being opposite the top side. Thus, claim 6 clearly recites the top side, including integrated circuit, and the rear side opposite the top side being perpendicular to the substrate.

Koike clearly teaches the flat, planar surfaces of the chip 3 as the top and rear sides. For instance, Koike notes, “the semiconductor chip 3, for instance, the silicon chip is mounted on the semiconductor chip mounting area while its face directed downward, electrodes on the

Amendment and Response Under 37 C.F.R. 1.116

Applicant: Michael Bauer et al.

Serial No.: 10/789,033

Filed: February 27, 2004

Docket No.: I431.103.101/FIN423US

Title: ELECTRONIC COMPONENT AND SEMICONDUCTOR WAFER, AND METHOD FOR PRODUCING THE SAME

semiconductor chip 3 not shown in the drawing are connected to the stud bumps 11....” Col. 11, ll. 42-48.

Moreover, the top and rear sides of a chip have particular meanings in the art. Generally, the rear side of the semiconductor chip is a portion of the rear side of a semiconductor wafer. The rear side of the semiconductor chip or wafer is distinguishable from the top side by its surface finish. The surface finish of the rear side is rougher and less polished than that of the top surface of the semiconductor chip or wafer, below which the integrated circuit structures are provided in the region of the chip body adjacent top surface. The side faces of the semiconductor chip are also identifiable and distinguishable from the top and rear sides since the semiconductor chip is singulated, typically by sawing, from the wafer creating a side face with a surface finish typical of the sawing process. Thus, as is accepted in the art, the rear and top sides of the semiconductor chip can only be particular sides so that the terms denote a particular identifiable side of the chip.

As such, Applicants respectfully submit claim 6, and all of the claims dependent on claim 6, are patentable over the combination of Nakajima and Koike.

CONCLUSION

As evidenced by the amendments and remarks presented above, Applicants have made a genuine effort to respond to each concern raised in the Advisory Action and the Final Office Action. The amendments presented are believed to place the application in condition for allowance. As this paper is presented with an RCE, the amendments and remarks are believed proper for consideration.

The commissioner is hereby authorized to charge Deposit Account No. 50-0471 for any fees that may be required in conjunction with this paper.

The Examiner is invited to contact the Applicant’s representative at the below-listed telephone numbers to facilitate prosecution of this application.

The Examiner is invited to contact the Applicant’s representative at the below-listed telephone numbers to facilitate prosecution of this application.

Amendment and Response Under 37 C.F.R. 1.116

Applicant: Michael Bauer et al.

Serial No.: 10/789,033

Filed: February 27, 2004

Docket No.: I431.103.101/FIN423US

Title: ELECTRONIC COMPONENT AND SEMICONDUCTOR WAFER, AND METHOD FOR PRODUCING THE SAME

Any inquiry regarding this Amendment and Response should be directed to Mark L. Gleason at Telephone No. (612) 767-2503, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja

Fifth Street Towers, Suite 2250

100 South Fifth Street

Minneapolis, MN 55402

Respectfully submitted,

Michael Bauer et al.,

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC

Fifth Street Towers, Suite 2250

100 South Fifth Street

Minneapolis, MN 55402

Telephone: (612) 573-2000

Facsimile: (612) 573-2005

Date: 06/08/2007

MLG:cjs

/Mark L. Gleason/

Mark L. Gleason

Reg. No. 39,998